Module Information	
Module Title	**Advanced Computer Architecture**
Module Code	**CSN502**

1. MODULE SUMMARY

Aims and Summary

This module is intended to understand the design principles and working of modern computer architectures and apply them to design processors of moderate instruction set complexity, identify performance bottlenecks and improve performance of I/O and memory. Students will be taught the principles and design of instruction sets, processor pipelines, cache systems & I/O systems and storage. Performance and design of RAID storage will be covered. Design of Networks on Chip, cache architectures and multicore processors will be emphasized. Students will be trained on the modelling and performance evaluation of computer architectures and their subsystems using computer architecture simulator software.

Module Size and Credits

Module size	Single
CATS points	12
ECTS credits	N/A
Open / restricted	Restricted
Availability on/off campus	On Campus/Off campus
Total student study hours	120
Number of weeks	4 weeks Full-time or 8 weeks Part-time.
Centre responsible	Centre for Computer Science and Engineering/Department of Electronics and Communication Engineering
Academic Year	2009

Entry Requirements (pre-requisites and co-requisites)

Normally to be qualified for entry to the Postgraduate Engineering Programme

Excluded Combinations

None

Composition of Module Mark (including weighting of components)

Full-time / Part-time : 50% Written Examination and 50 % Assignment

Pass Requirements

A minimum of 40 % marks in the written examination and a minimum of 40% marks in the assignment are required for a pass and overall 40% marks

Special Features

80% attendance in theory and 80% attendance in laboratory are required.
It is likely that considerable time will be spent in School facilities outside of normal timetabled class time.

Courses for which this module is mandatory

M.Sc. [Engg] in Computer Science and Networking

Courses for which this module is a core option

None

2. TEACHING, LEARNING AND ASSESSMENT

Intended Module Learning Outcomes

After undergoing this module, students will be able to:

1. Explain the design principles and working of modern computer architectures and their subsystems
2. Design a RISC instruction set of moderate complexity and cache subsystems of minimal latency for specified requirements
3. Design and implement pipelined processors of moderate complexity using the optimised instruction set
4. Use the appropriate software tools to model and evaluate computer architectures and their subsystems

Indicative Content

Class Based Sessions

1. **Review:** Types of processors, their architectures and evolution, Program execution cycle, Addressing modes and register organization, instruction sets and assembler programming**,**, Microcoded processors, Pipelining, Memory and its hierarchy, Buses and processor interconnects, ALU, Number representation systems, Computer classes and architectures, Multicore processors
2. **Design of Instruction Sets and Microcoded Processors:** Instruction sets and snstruction set architecture for a embedded processor, Instruction set optimization, Microcoded control, Microinstruction formats, Horizontal vs Vertical microcoded processors, VLIW and Superscalar processors
3. **Pipelining and Design of Pipelined Processors:** Fundamental concept of pipelining, Typical architecture of Pipelined Processors, Power savings due to pipelining, Design of pipelines using Davidson diagrams, Pipeline hazards, Avoidance of pipeline hazards using Tomasulu algorithm and register scoreboarding
4. **Architecture and Design of Floating Point Units (FPUs) and CORDIC:** Importance of FPUs, Design considerations for FPUs, Floating point implementation of addition, subtraction, multiplication and division algorithms, Performance considerations of FPUs, CORDIC processor
5. **Architecture and Design of Cache Memory:** Effect of cache architecture and size on performance, Hit rate and miss rate, Direct mapped and set-associative caches, write through and write back caches, Cache coherency and cache coherency protocols for single core and multicore processors, Shared and non-shared caches, Cache replacement algorithms, Cache line size, Performance measurement of cache memories
6. **Storage and RAID Architectures:** Current state of Disk storage, RAID concepts, RAID levels from 0 to 6, Storage interfaces, Network Attached Storage (NAS) architectures, Data security in NAS
7. **I/O Design and Inter-Processor Communication**: Taxonomy of IO structures, Buses, Rings, NOC and SERDES, Electrical design issues in buses – power, reflection, Bus arbitration schemes, Network on chip (NOC) design considerations, Optical interconnect for multicore processors
8. **Multicore Processors and Design of Multicore Processors:** Heterogenous and homogenous multicore processors, Threads and multithreading, load balancing and barrier synchronization on multicore, Operating systems for homogenous and heterogenous multicore, Local vs. global cache and cache coherency techniques in multicores, Power management for multicore, Performance measures and bottlenecks for multicore processors
9. **Data dependencies, Parallel Processing and Parallelisation:** Data dependencies in a program and their importance for a processor and compiler design, RAW, WAR and WAW dependencies, Data Dependency Graphs, Compilers and data dependencies, Data dependency analysis in parallel computing, Program dependencies, Particle type and continuum type parallel problems, Critical sections of code, Parallel and Serial portions of a program, Loop parallelization
10. **Summary and Trends in Computer Organization:** The multicore processing landscape, Trends in processor architecture at 45 nm process nodes, Transactional memory for cache coherency, Massively parallel fine grained processors, Multicore processors with optical interconnect

Laboratory Based Sessions

1. Introduction to the HASE architectural simulator and simulation of a simple load store micro-coded processor architecture in HASE
2. Implement Multiply and ADD on the EMMA module and simulate using HASE environment
3. Implement simple single stage multiply accumulate instruction in EMMA
4. Understand the HASE simulation model for MIPS processor code. Run pipelined operations on MIPS pipeline using HASE. Visualize the pipeline operations in HASE

5. Simulation of pipeline hazards in MIPS processor model using HASE
6. Demonstrate the operations of the Memory unit in MIPS processor using HASE
7. Lab explaining and demonstrating Tomasulo algorithm for register renaming in HASE
8. Simulation of Cache model with 2 levels of hierarchy in HASE

Teaching and Learning Methods

1. Theoretical Knowledge [~30% of module time]
   a. Face to face lectures from a module leader- 30 hours
   b. Case study teaching and discussion from a practicing engineer- 6 hours

36 hours

2. Laboratory Practice (Skills) [~ 25% of module time]

30 hours

3. Application Orientation and Problem Solving [45% of module time]
   a. Reading
   b. Research
   c. Written Examination
   d. Assignment Solving and Documentation

54 hours

Method of Assessment

Part-A

Written Examination [50% Weighting]

At the end of the module, normally on the last day of the last week of the module, written examination is conducted to test students' understanding of taught theoretical concepts. The question paper will comprise either or a combination of the following:

- 6 questions, out of which 5 questions need to be answered
- Practical laboratory work
- Presentations
- Field work
- Creation of a physical model

The marks scored by the student will be scale down to 50% weight.

Part –B

Assignment [50% Weighting]

Students are required to submit word processed assignment report on formally announced last day of the module. Assignment tests students' problem solving skills based on taught concepts. The assignment is assessed for 100 marks but scored marks is scaled down to 50%

Assessment				
Learning Outcomes	**1**	**2**	**3**	**4**
Part A	**X**	**X**	**X**	
Part B	**X**	**X**	**X**	**X**

Both written examination scripts and assignment reports will be double marked/valued

Re-assessment

A minimum of 40 % marks in the written examination and a minimum of 40% marks in the assignment are required for a pass in the module.
A student failing in any one of the components or both is considered as FAIL in the module. A failed student is required to retake the module at the next opportunity. A maximum of 3 attempts including the original are allowed.

Date of Last Amendment

May 2009

3. MODULE RESOURCES

Essential Reading

1. Module Notes

Recommended Reading

Books

1. John Hennessy and David Patterson, *Computer Architecture: A Quantitative Approach*, 4th edition, Morgan Kaufmann, 2007
2. Bruce Jaocb, Spencer Ng and David Wang, *Memory Systems - Cache, DRAM, Disk*, Morgan Kaufmann, 2008
3. Sudeep Parischa and Nikhil D. Dutt, *On-Chip Communication Architectures: System on Chip Interconnect*, Morgan Kaufman, 2008
4. Hesham El-Rewini and Mostafa Abd El-Barr, *Advanced Computer Architecture and Parallel Processing,* John Wiley, 2005
5. Maurine Herlihy and Nir Shavit, *The Art of Multiprocessor Programming*, Morgan Kaufmann, 2008
6. V. Heuring and H. Jordan, *Computer Systems Design and Architecture,* Pearson Education, 2006
7. Robert P. Colwell, *The Pentium Chronicles: The People, Passion, and Politics Behind Intel's Landmark Chips,* Wiley, 2006
8. Dezso Sima and Terence Fountain, *Advanced Computer Architectures – A Design Space Approach*, 3rd edition, McGraw-Hill, 2001
9. Harold Stone, *High Performance Computer Architecture*, 3rd edition, Addison-Wesley, 1993
10. Brett Olsson, *A developers guide to the Power Architecture*, IBM Press, 2004
11. David Seal, *ARM Architecture Reference Manual*, Addison-Wesley, 2004

Journals

1. IEEE Transactions on Computers
2. IEEE Transactions on VLSI systems
3. Proceedings of the IEEE

Magazines

1. IEEE Signal Processing Magazine
2. IEEE Micro

Internet Sites

1. http://www.xilinx.com
2. http://www.edn.com
3. http://www.ocpip.com
4. http://www.arm.com
5. http://www.ddj.com
6. http://pages.cs.wisc.edu/~arch/www/

Laboratory

Hardware: PCs

Software: HASE architectural simulator

Software Manual:

4. MODULE ORGANISATION

Module Leader

Name	Mr. Dipayan "Tim" Mazumdar
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Date and Time of Examination

As per time table

Subject Quality and Approval Information

Subject Quality Group / Subject Board	Electronics and Communication Engineering
Subject Assessment Board	Postgraduate Engineering Programmes
Shortened title	CARCH
Date of approval by MARP	May 2009