1. MODULE SUMMARY

Aims and Summary
This module prepares the students to analyze and design MOS integrated circuits. A strong theoretical background of MOS transistors and device characterization is imparted to the students along with emphasis on their design and analysis. Design of memory circuits, data path operators & other complex CMOS macros for timing, low power and area are discussed with relevant case studies. Students will be required to use industry standard EDA tools HSPICE, Nanosim and Cadence Virtuoso to build, optimize and simulate Micro and Macro blocks for designing integrated circuits.

Module Size and Credits

<table>
<thead>
<tr>
<th>Module size</th>
<th>Single</th>
</tr>
</thead>
<tbody>
<tr>
<td>CATS points</td>
<td>10</td>
</tr>
<tr>
<td>ECTS credits</td>
<td>N/A</td>
</tr>
<tr>
<td>Open / restricted</td>
<td>Restricted</td>
</tr>
<tr>
<td>Availability on/off campus</td>
<td>On Campus/Off campus</td>
</tr>
<tr>
<td>Total student study hours</td>
<td>100</td>
</tr>
<tr>
<td>Number of weeks</td>
<td>5 weeks Full-time or 8 weeks Part-time.</td>
</tr>
<tr>
<td>Department responsible</td>
<td>Department of Electronics and Electrical Engineering</td>
</tr>
<tr>
<td>Academic Year</td>
<td>2012</td>
</tr>
</tbody>
</table>

Entry Requirements (pre-requisites and co-requisites)
Normally to be qualified for entry to the Postgraduate Engineering Programme

Excluded Combinations
None

Composition of Module Mark (including weighting of components)
Full-time / Part-time : 50% Written Examination and 50% Assignment

Pass Requirements
A minimum of 40% marks in the written examination and a minimum of 40% marks in the assignment and an overall 40% marks is required for a pass

Special Features
80% attendance in theory and 80% attendance in laboratory are required.
It is likely that considerable time will be spent in School facilities outside of normal timetabled class time.

Courses for which this module is mandatory
M.Sc. [Engg.] in VLSI System Design

Courses for which this module is a core option
M.Sc. [Engg.] in Technology and Engineering Management
2. TEACHING, LEARNING AND ASSESSMENT

Intended Module Learning Outcomes
After undergoing this module students will be able to:

1. Explain the theoretical concepts and characterize MOS transistors, micro and macro MOS circuits
2. Apply theoretical concepts to design CMOS circuits and analyze their static and dynamic properties
3. Design, model, optimize and verify complex CMOS macros for timing, low power and area
4. Proficiently use industry standard Synopsys and Cadence tools to design and analyze integrated circuits

Indicative Content

Class Room Lectures

a. MOS transistor theory: Introduction, structure, operation of enhancement and depletion type MOS transistor, current-voltage characterization of MOS transistor, biasing of MOS transistor, small signal model of MOS transistor, second order effect- body effect, channel length modulation, subthreshold effect, hot electron effect, tunnelling, punch through. MOS transistor capacitances, model parameters, different level of MOS model equations, modelling of MOS transistors using SPICE and scaling of MOS transistors. 65nm, 45nm, 38nm, 22nm design challenges. Case study of modelling MOS devices and extracting model parameters.

b. CMOS inverter design: Introduction, types MOS inverter, resistive load inverter, depletion load inverter, CMOS inverter, design of CMOS inverter, DC (static) characteristic analysis - voltage transfer characteristic and noise margin. Transient (dynamic) analysis - propagation delay, rise time and fall time calculation. CMOS inverter static and dynamic power, CMOS inverter load capacitance and interconnection parasitic. Case study of CMOS inverter design for noise margin, speed, power and timing

c. Combinational and sequential CMOS logic circuits: Introduction, CMOS logic circuits, complex logic circuits, clocked CMOS logic, pass transistor logic, CMOS transmission gates, problems of charge sharing, precharging techniques. Behaviour of bistable elements, timing metrics, SR latch and flip-flop circuits, mux based latches, clocked latch and flip-flop circuit. Case study of combinational and sequential circuits for timing, area and power

d. Logical effort: Introduction, transistor sizing, delays in CMOS logic gates, fan-in and fan-out consideration, fast complex gate techniques, computing of logical effort, path and branch effort, multistage delay and best stage effort. Case study of CMOS circuit design using logical effort.

e. Memory design: Introduction, need for memories, classification of memories, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), memory architectures, 6T SRAM memory cell architecture, peripheral memory circuitry - sense amplifier, read/write circuitry, bit line precharge circuitry, row and column decoders and memory timing.

f. Data path subsystem: Introduction, arithmetic logic circuits, classification of adders, design of mirror adder, ripple carry adder, Manchester carry chain adder, carry skip adder, comparison of adders, multipliers and shifters. Case studies of data path sub-systems.

g. Low Power CMOS design: Introduction, power dissipation, static and dynamic power dissipation, techniques for reduction of power dissipation, low
power design through voltage scaling, estimation and optimization of switching activity, reduction of switched capacitance. Case study of optimizing power in CMOS circuits.

**Laboratory Practice**

1. Model and characterization of MOS transistor using HSPICE
2. Design and analysis of CMOS inverter (static and transient characteristic analysis)
3. Design and analysis of combinational CMOS circuits using HSPICE and Spectre
4. Design and analysis of sequential CMOS circuits using HSPICE and Spectre
5. Transistors sizing and analysing of complex CMOS circuit using logical effort method
6. Build the memory cell architectures using Cadence Virtuoso
7. Memory peripheral circuit design
8. Build data path subsystems – Adders
9. Build data path subsystems – Multiplier and shifters
10. Design and analysis of low power CMOS circuits

**Teaching and Learning Methods**

1. Theoretical Knowledge
   a. Face to face lectures

2. Laboratory Practice (Skills)

3. Application Orientation and Problem Solving
   a. Reading
   b. Research
   c. Written Examination
   d. Assignment Solving and Documentation
Method of Assessment

Examination [50% Weightage]

1. Viva/Presentation on a specified topic ........................................... (10%)
2. Student performance on classroom tests .................................... (10%)
3. Written examination ................................................................ (30%)

Part –B

Assignment [50% Weightage]

Students are required to submit a word processed assignment report.

<table>
<thead>
<tr>
<th>Assessment</th>
<th>Learning Outcomes</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part A</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Part B</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Both written examination scripts and assignment reports will be double marked.

Re-assessment

A minimum of 40% marks in the written examination and a minimum of 40% marks in the assignment are required for a pass.

A student failing in any one of the components or both is considered as FAIL. A failed candidate is required to re-register for the module in the next offering. A maximum of 3 attempts including the original are allowed.

Date of Last Amendment

November 2011

3. MODULE RESOURCES

Essential Reading

1. Module Notes

Recommended Reading

Books

Journals
1. IEEE Transactions on Solid State Circuits
2. IEEE Transactions on Circuits and Systems
3. VLSI Journal, Elsevier

Magazines

Internet Sites
1. www.berkeley.edu (accessed on 18th January 2012)
2. www.mosis.com (accessed on 18th January 2012)
3. www.eetimes.com (accessed on 18th January 2012)

Laboratory

Hardware: Workstations

Software: Synopsys HSPICE, Cadence Virtuoso, Nanosim, Cadence Pspice, LTspice, Microwind.

Software Manual: HSPICE and Virtuoso manuals

4. MODULE ORGANISATION

Module Leader

Name: Dr. Cyril Prasanna Raj, P
Room: B402-1
Telephone number: 080-4906 5555 (Extn. 2325)
E-mail: cyril@msrsas.org

Date and Time of Examination

As per time table

Subject Quality and Approval Information

Subject Quality Group / Subject Board: Electronics and Electrical Engineering
Subject Assessment Board: Postgraduate Engineering and Management Programmes
Shortened title: ICAD
Date of approval by MARP: November 2011